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FABRICATION OF ORGANIC THIN FILM TRANSISTORS USING LAYER-BY-LAYER ASSEMBLY (PREPRINT)

Jeffery T. Stricker, Anna D. Gudmundsdóttir, Adam P. Smith, Barney E. Taylor, and Michael F. Durstock

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AIR FORCE MATERIEL COMMAND
WRIGHT-PATTERSON AIR FORCE BASE, OH 45433-7750**

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*//Signature//   //Signature//
MICHAEL F. DURSTOCK, Project Engineer   JOHN F. MAGUIRE, Chief
Polymer Branch   Polymer Branch
Nonmetallic Materials Division   Nonmetallic Materials Division

//Signature//
SHASHI K. SHARMA, Acting Deputy Chief
Nonmetallic Materials Division
Materials and Manufacturing Directorate

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Jeffery T. Stricker and Anna D. Gudmundsdóttir (University of Cincinnati)
Adam P. Smith (UES, Inc.)
Barney E. Taylor (University of Dayton Research Institute)
Michael F. Durstock (AFRL/MLBP)

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7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

University of Cincinnati
Cincinnati, OH 45221-0012

UES, Inc.
Beavercreek, OH

University of Dayton Research Institute
300 College Park
Dayton, OH 45469

Polymer Branch (AFRL/MLBP)
Nonmetallic Materials Division
Materials and Manufacturing Directorate
Air Force Research Laboratory, Air Force Materiel Command
Wright-Patterson Air Force Base, OH 45433-7750

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14. ABSTRACT
Layer-by-layer assembly is presented as a deposition technique for the incorporation of ultra-thin gate dielectric layers into thin-film transistors utilizing a highly doped organic active layer. This deposition technique enables the fabrication of device structures with a controllable gate dielectric thickness. In particular, devices with a dielectric layer comprised of poly(allylamine hydrochloride)/poly(acrylic acid) (PAH/PAA) bilayer films were fabricated to examine the properties of poly(3,4-ethylenedioxythiophene):poly(styrene sulfonate) (PEDOT:PSS) as the transistor active layer. The transistor Ion/off ratio and switching speed are shown to be controlled by the gate bias, which is dependent upon the voltage applied and the number of bilayers deposited for the gate dielectric. The devices operate in the depletion mode as a result of de-doping of the active layer with the application of a positive gate bias. The depletion and recovery rate are highly dependent on the level of hydration in the film and the environment under which the device is operated. These observations are consistent with an electrochemical de-doping of the conducting polymer during operation.

15. SUBJECT TERMS
PEDOT:PSS, layer-by-layer assembly, thin film transistors, ultra-thin gate dielectric

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Introduction

Organic thin-film transistors (TFTs) have received considerable attention as a low-cost, light-weight, flexible alternative to traditional amorphous silicon devices in a variety of applications.[1,2,3,4] Some specific examples include large area flat-panel displays, sensor arrays, and smart cards. Previous studies have investigated the use of a number of materials for both the active layer and the gate dielectric in various TFT architectures. These efforts have highlighted the critical roles that interface effects,[5,6] material properties,[7,8] and processing[9] play in determining device performance.

Conjugated small molecules, such as pentacene, or polymers, such as poly(3-hexylthiophene), are commonly used as the active layer in organic TFT architectures.[10,11] These materials are chemically undoped, but have relatively high charge carrier mobilities that permit their use as the active layer in thin film transistors based on a field effect. Other types of transistor devices have also been studied, though to a lesser extent. Electrochemical transistors have been reported by Wrighton[12,13,14,15,16] and others[17,18,19] and are commonly laterally arranged devices with a conjugated polymer whose redox state is modified by a gate bias. In addition, MacDiarmid[1] and Epstein[2,20,21,22] have reported on devices using the doped conjugated polymer system poly(3,4-ethylenedioxythiophene):poly(styrene sulfonate) (PEDOT:PSS) as the active layer. In both of these device configurations, the observed response times are generally quite slow (seconds to minutes). Clearly these devices do not compete with the more typical 'solid state' transistors, however their investigation impacts the broader context of sensors, molecular and flexible electronics, and fundamental materials chemistry.

The operating mechanism of devices based on PEDOT:PSS is still not completely understood, although it is generally believed that the observed effect is related to ion motion under an applied field.[21] However, the nature of how this phenomenon effects a change in conductivity is still under consideration. Possibilities that have been suggested include the existence of a metal-insulator transition[20] or an electrochemical de-doping effect similar to that discussed above.[17,18] In this communication, we address these issues by reporting on some fundamental characteristics of devices fabricated with careful control over the gate dielectric thickness and the environment under which the device is operated. The means by which we achieve precise control over the gate dielectric thickness is by using an electrostatic, layer-by-layer deposition procedure. This technique can be used to deposit extremely thin, pinhole-free films over large, non-uniform surfaces,[23] and has been studied in great detail for use in surface modification layers,[24,25] membranes,[26] and device applications.[27,28] By alternately dipping a substrate between two dilute polyelectrolyte solutions of opposite charge (i.e., a polycation and a polyanion), a thin film is built up due to the electrostatic interactions between the polyelectrolytes. In this study, the layer-by-layer approach was used to deposit ultra-thin gate dielectric layers comprised of PAH/PAA bilayers with a controllable thickness. By combining this method with the use of a conductive polymer active layer, we present additional insight into the nature of how these TFT devices operate. Furthermore, this thin film deposition approach can be broadly applicable to other transistor designs using a variety of different device configurations and alternative active and dielectric layer materials, as will be reported in a separate communication.

Experimental

Aqueous stock solutions of PEDOT:PSS, under the tradename of Baytron® P with a reported concentration range of 1 – 5%, were purchased from H.C. Stark Inc. and filtered with 1 μm pore size filters prior to use. Spin-coated films of PEDOT:PSS were prepared with solutions comprised of an 80:20 (by weight) mixture of the aqueous Baytron P stock solution with ethylene glycol, respectively, with a small amount (< 1 %) of dodecabenzene sulfonic acid. The films were fabricated by spin-coating at 500 rpm for 10 s and then 3000 rpm for 60 s. Polyelectrolyte solutions (10 mM) were pH-adjusted with NaOH and HCl using an Orion model 230A pH meter. Each monolayer deposition cycle (~ 15 min) was followed by multiple rinse steps in deionized (18 MΩ·cm) H_2O in a Carl Zeiss Microm DS-50 automatic slide stainer. Silver and aluminum electrodes were thermally evaporated at a rate of 3 and 4 – 5 Å/s, respectively, in an Explorer 18 Denton Vacuum system (< 10^{-7} Torr) using a Telemark model 860 deposition controller. Film thicknesses were measured with a Tencor P-10 surface profiler at a stylus force of 0.6 mg. The absorbance spectra were obtained using a Varian Cary 5000 UV-Vis-NIR spectrophotometer. The van der Pauw technique was used to determine film resistivity with a Keithley 4200 semiconductor characterization system. The size of the active channel was approximately 2 mm wide by 3 mm long. The TFT device performance was characterized with two Keithley 2400 SourceMeters.® The $I_{DS} – V_{DS}$ characteristics were obtained with a V_{DS} dwell time of 10 seconds and a V_G dwell time of 60 seconds and the $I_{DS} – time$ characteristics were obtained using a V_{DS} of 0.1 V. The $I_{on/off}$ ratios obtained from the data for V_G = 2.0 and 2.5 V were calculated after adjusting the curves to pass through the origin to account for the effects caused by the device leakage current at these

low I_{DS} values. Nitrogen was bubbled through deionized water (18 MΩ·cm) to create humidified N_2 conditions in the test chamber (relative humidity ~ 75 %). More precisely controlled humidity conditions were obtained by performing experiments in a SH-241 ESPEC bench-top type temperature and humidity chamber purged with N_2.

Results and Discussion

A schematic representation of the TFT device configuration used in this study is provided in Figure 1. Bilayers of poly(allylamine hydrochloride) (PAH), the polycation, and poly(acrylic acid) (PAA), the polyanion, were deposited onto an evaporated aluminum gate electrode (350 – 400 Å) through layer-by-layer assembly to obtain a gate dielectric of controllable thickness. The films were then heat-treated at 235 °C for 4 hours under dry N_2 to chemically crosslink the film to improve stability and impermeability.[29,30] After spin-coating a PEDOT:PSS layer directly onto the assembled dielectric layer, silver source and drain electrodes were vapor deposited on opposite sides of the active channel to complete the device. The PEDOT:PSS active layer thickness varied from 500 – 900 Å, while conductivities ranged from 65 to 75 S/cm. This bottom gate arrangement was utilized to avoid degradation of the conducting polymer layer during heat treatment of the gate dielectric.

Representative performance characteristics are shown in Figure 2 for a device with a gate dielectric comprised of 10 PAH/PAA bilayers deposited at a pH of 6 to 6.5 that was tested under ambient conditions. Under these conditions, the total thickness of the gate dielectric was approximately 30 Å, which corresponds to an individual bilayer thickness of about 3 Å, consistent with that reported by Shiratori et al.[31] As expected, the

application of a positive gate bias resulted in a slow decrease of the source-drain current (I_{DS}) for these devices. Figure 2a shows that as the gate bias was gradually increased from 1.0 to 2.5 V, the device exhibited a higher $I_{on/off}$ ratio, a faster depletion rate, and a recovery rate that was much slower than the depletion rate and relatively independent of gate bias. These trends are shown explicitly in Figure 2b whereby the $I_{on/off}$ ratio was calculated from the change in I_{DS}, the depletion rate was characterized by the initial slope (obtained 3 s after the gate bias was applied) of the I_{DS} – *time* curve, and the recovery rate was characterized by the slope of the I_{DS} – *time* curve at 10 μA during recovery. Furthermore, the gate current (I_G) exhibited an initial increase upon application of the gate bias, and then decreased exponentially until the gate bias was removed. In all cases, the I_G decreased to several orders of magnitude less than the initial I_{DS}. In addition, the magnitude and time dependence of the gate current are significantly higher than a simple capacitive charging current due to the gate dielectric. All of these trends are consistent with an electrochemical de-doping effect of the PEDOT:PSS and this will be discussed later in greater detail. It should also be noted that upon prolonged application of the gate bias in an ambient environment (data not shown), the aluminum gate can become electrochemically oxidized, which can affect the observed $I_{on/off}$ ratio, switching speed, and overall device performance. Care should be taken to avoid these effects.

The thickness of the gate dielectric can be precisely tuned simply by changing the number of PAH/PAA bilayers deposited. As shown in Figure 3, both the $I_{on/off}$ ratio and the depletion rate continuously decreased as the number of bilayers was increased from 10 to 40 (film thickness = 30 to 130 Å) with a constant V_G of 2.0 V. Furthermore, when the deposition conditions of the PAH/PAA bilayer film were changed such that much
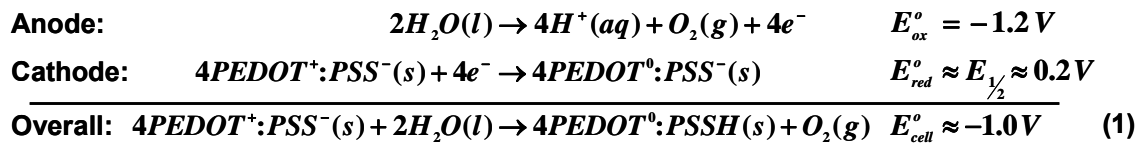
thicker gate dielectric layers than those shown were obtained, a significant decrease in the switching speed was observed. Specifically, when the pH of both polyelectrolyte deposition solutions was set to 3.5, a 40 bilayer PAH/PAA film had a thickness of 2400 Å. Using this film as the gate dielectric resulted in a device with a depletion rate four orders of magnitude lower than the comparable devices shown in Figure 3. Only when the gate bias was increased to approximately 20.0 V did the depletion rate approach that observed for the devices shown in Figure 3. This trend in switching speed is consistent with previously reported values for similar TFTs utilizing an optical adhesive or a thin spin-coated film of poly(4-vinylphenol) as the gate dielectric.[1,20,21] The $I_{on/off}$ ratios, however, were significantly lower, possibly due to the use of a top gate electrode architecture, interface effects, or different environmental test conditions. It should also be noted that devices with no PAH/PAA layer did function to a limited extent, suggesting that the native aluminum oxide layer $(2 - 3 \text{ nm})$[32] can serve as the gate dielectric. Indeed, aluminum oxide has previously been used as the dielectric layer, but only at much greater thicknesses $(26 - 130 \text{ nm})$.[33]

Due to the fact that the operating mechanism of these devices is believed to be related to ion motion under the applied field, it is expected that the level of hydration of these films will significantly influence their performance characteristics. In addition to testing under ambient conditions as described above, TFT devices were tested under both dry and humidified N_2 conditions. Representative $I_{DS} - V_{DS}$ characteristics obtained for a device with 40 PAH/PAA bilayers as the gate dielectric, under humidified N_2 conditions, are presented in Figure 4a. An approximately linear relationship was observed in all cases with a minor deviation around the origin, likely due to effects caused by ongoing

depletion, ion drift within the film, or cross-talk between the electrodes. The $I_{on/off}$ ratios (at V_{DS} = 0.1 V) were significantly higher than those shown previously obtained under ambient conditions and agree with other reported values.[1,20,21] The same general trends as those discussed above for increasing gate voltage and decreasing dielectric thickness were observed for devices tested under humidified N_2 conditions. Figure 4b illustrates the effects that the test environment has on the performance characteristics of this device by showing I_{DS} as a function of gate bias under different test conditions. By comparing the data taken under ambient conditions (relative humidity (RH) ~ 30 − 40%) to those taken under humidified N_2 conditions (RH ~ 75%), it can be seen that the higher level of humidity not only caused a higher $I_{on/off}$ ratio, but also induced the device to switch at lower voltages. Surprisingly, when the device was operated in a dry environment, effectively no change in the I_{DS} was observed with V_G. In other words, the device switching behavior was completely inhibited when moisture was removed from the film.

To further probe this effect, device testing was performed under carefully controlled humidification conditions in a separate humidity chamber. Figure 5 shows the results for a device with 10 PAH/PAA bilayers as the gate dielectric tested under a RH value ranging from 0 to 75%. Both the $I_{on/off}$ ratio and the depletion rate systematically increased with RH, consistent with the results above. Apparently, the incorporation of moisture into the film is required for these devices to operate and better device performance is obtained with higher moisture content. This requirement is emphasized by the fact that if N_2 was bubbled through anhydrous methanol or ethanol (instead of water) before exposing it to the device, the effect was the same as with dry N_2. That is to say, the device switching behavior was inhibited.

As mentioned above, the observed device behavior is consistent with an electrochemical de-doping of the PEDOT:PSS during device operation. Due to the dependence of the device performance on water content, equation (1) is presented as a description of the way in which the device operates. With a positive V_G, the aluminum gate electrode (see Figure 1) serves as the anode at which the oxidation of water occurs to generate $O_2(g)$. It should be noted that crosslinked PAH/PAA multilayers have been shown to passivate aluminum.[34] The source electrode then serves as the cathode at which the oxidized $PEDOT^+$ molecules are reduced back to their neutral species (i.e. de-doped). The protons generated at the anode can subsequently migrate through the polyelectrolyte multilayer gate dielectric film to produce SO_3H at the cathode. Consequently, a higher gate bias results in a faster depletion rate and a larger $I_{on/off}$ ratio due to a larger driving force for ion migration and PEDOT de-doping. Similarly, using a thicker gate dielectric (more PAH/PAA bilayers) results in both a smaller depletion rate and $I_{on/off}$ ratio due to a reduction of the effective electric field. Water must be present for oxidation, otherwise operation is inhibited, as observed.

$$\text{Anode:} \qquad 2H_2O(l) \rightarrow 4H^+(aq) + O_2(g) + 4e^- \qquad E^o_{ox} = -1.2\,V$$

$$\text{Cathode:} \qquad 4PEDOT^+{:}PSS^-(s) + 4e^- \rightarrow 4PEDOT^0{:}PSS^-(s) \qquad E^o_{red} \approx E_{1/2} \approx 0.2\,V$$

$$\text{Overall:} \quad 4PEDOT^+{:}PSS^-(s) + 2H_2O(l) \rightarrow 4PEDOT^0{:}PSSH(s) + O_2(g) \quad E^o_{cell} \approx -1.0\,V \qquad (1)$$

The recovery behavior of the device was described above as being independent of the gate bias applied. Upon removal of the gate bias, the reaction equilibrium favors the doped form of PEDOT and so the rate of recovery is solely dependent upon this reverse reaction rate. Given enough time, however, the $O_2(g)$ that is generated during depletion will diffuse out of the film thereby prohibiting the back reaction (i.e. recovery) when the gate bias is removed. This effect is illustrated in Figure 6 for a device with 10 PAH/PAA

bilayers as the gate dielectric tested under humidified N_2 conditions. By applying a gate bias of 1.5 V, the device becomes completely depleted ($I_{on/off}$ ratio ~ 10^3) in approximately 4.5 minutes. If the gate bias were to be removed at this point, the device would immediately begin to recover as demonstrated above. However, the gate bias is maintained at 1.5 V for 12 minutes. When the gate bias was removed after this time, the device effectively failed to recover and remained in the "off" state even though the gate bias had been removed. This effect is simply due to the fact that the $O_2(g)$ generated during depletion has diffused out of the film thereby prohibiting the back reaction (1) when the gate bias is removed. If the device is subsequently exposed to $O_2(g)$ again (at time ~ 45 min in Figure 6), the device immediately begins to recover at a rate that is consistent with that shown above under ambient conditions. Similar types of electrochemical effects have been demonstrated for PEDOT:PSS using laterally arranged devices and an electrolyte.[18,19] Additionally, the electrolysis of water is known to change the doping level of conjugated polymers[35] and is suspected of forming black spots in LEDs by reducing the PEDOT.[36]

To provide further evidence for this electrochemical de-doping mechanism, TFT devices were made using indium tin oxide (ITO) as a transparent gate electrode in order to investigate the optical properties of the active layer *in-situ*. Other than the use of this transparent gate electrode, the devices had the same architecture and operated with the same trends as previously discussed. The absorption spectra shown in Figure 7 were obtained for a device with ITO as the gate electrode and 40 PAH/PAA bilayers as the gate dielectric. The initial spectrum obtained before the application of a gate bias (V_G = 0.0 V) under humidified N_2 conditions clearly indicates the presence of doped PEDOT

with broad peaks present at 965 nm and beyond 1500 nm, which are representative of the subgap states for the polaron and bipolaron charge carriers.[37],[38] In addition, the small peak at 650 nm corresponds to the $\pi \rightarrow \pi^*$ transition in undoped PEDOT. Upon application of a gate bias ($V_G = 4.0$ V), the broad peak beyond 1500 nm decreases with a corresponding increase in the peaks at 965 nm and 650 nm. These spectral changes are consistent with a reduction in the doping level of the PEDOT[39] upon application of a positive gate bias. While the exact nature of the de-doping process is not completely understood, a multi-step electron transfer process has previously been reported to account for changes in the doping level of PEDOT and the associated changes in spectral features.[40]

Upon removal of the gate bias, the device starts to recover and the spectral features tend toward their initial, doped state. The initial recovery in a humidified N_2 environment (thin solid lines in the figure) is likely due to $O_2(g)$ remaining in the film, but this recovery becomes arrested and full recovery (re-doping) can only be obtained when the device is exposed to the ambient (i.e. O_2) environment (thin dashed lines).

Conclusions

The incorporation of ultra-thin polymer dielectric layers into TFT devices has been demonstrated using a layer-by-layer assembly deposition technique. The $I_{on/off}$ ratio and depletion rate for these devices increased with either a higher gate bias or a lower dielectric thickness. An electrochemical mechanism involving water oxidation and PEDOT$^+$ de-doping (i.e. reduction) was presented as the depletion mechanism for these devices. The fact that moisture is required for depletion, $O_2(g)$ is needed for recovery,

and the recovery rate is independent of the gate bias, all support this mechanism. The spectral evidence of de-doping and re-doping of the active layer is also in agreement with the proposed mechanism. While layer-by-layer deposition of the gate dielectric has been demonstrated for transistors based on doped, conducting polymer layers, it is also applicable to other types of transistor architectures in which ultra-thin, pin-hole free gate dielectrics are desirable, as will be discussed in a separate report.

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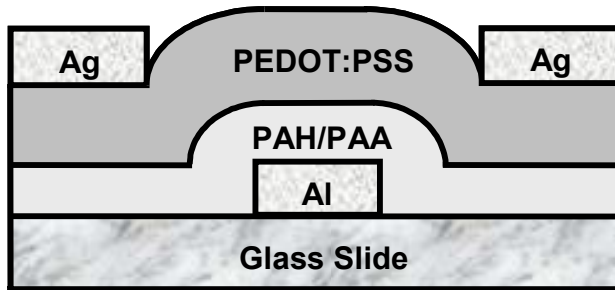
Captions for Figures

Figure 1. Schematic, bottom gate architecture of a TFT device with PEDOT:PSS as the active layer, PAH/PAA as the gate dielectric layer, silver as the source and drain electrodes, and aluminum as the gate electrode.

Figure 2. a) Performance characteristics of a TFT device tested under ambient conditions. The gate dielectric layer consisted of 10 PAH/PAA bilayers (deposited at a pH of 6.5) with a total thickness of ~ 30 Å. b) Depletion rate (▲), recovery rate at $I_{DS} = 10$ μA (♦), and $I_{on/off}$ ratio (□) as a function of gate bias for the devices shown in (a).

Figure 3. Depletion rate (▲) and $I_{on/off}$ ratio (□) as a function of the number of PAH/PAA bilayers deposited as the gate dielectric at a pH of 6.5. Devices were tested at $V_{DS} = 0.1$ V under ambient conditions with the application of a 2.0 V gate bias.

Figure 4. a) $I_{DS} - V_{DS}$ characteristics (at $V_{DS} = 0.1$ V) of a device tested under a humidified N_2 environment with a gate dielectric layer comprised of 40 PAH/PAA bilayers deposited at a pH of $6 - 6.5$ (thickness = 130 Å). b) $I_{DS} - V_G$ characteristics (at $V_{DS} = 0.1$ V) for this device tested under dry N_2 (♦), ambient (■), and humidified N_2 (▲) conditions.

Figure 5. Depletion rate (▲) and $I_{on/off}$ ratio (□) (measured at $3 - 5$ seconds and 260 seconds after application of the gate bias, respectively) for a device tested under a range of relative humidities at a gate bias of 1.25 V and having a gate dielectric comprised of 10 PAH/PAA bilayers deposited at a pH of $6 - 6.5$ (thickness = 30 Å).

Figure 6. Time-dependent performance characteristics (at V_{DS} = 0.1 V) of a TFT device with a gate dielectric comprised of 10 PAH/PAA bilayers deposited at a pH of 6 – 6.5 (thickness = 30 Å). Testing was initially done under humidified N_2 conditions and switched to ambient conditions after 45 minutes.

Figure 7. Absorption spectra obtained *in-situ* during operation of a device with an ITO gate electrode and a gate dielectric comprised of 40 PAH/PAA bilayers deposited at a pH of 6 – 6.5 (thickness = 130 Å). Spectra were obtained under humidified N_2 conditions before (thick grey line) and after (thick black line) a gate bias of 4.0 V was applied. During recovery, spectra (taken at 280 s intervals) were obtained first under humidified N_2 conditions (thin solid lines) and subsequently under ambient conditions (thin dashed lines).

Figures

Figure 1. Schematic, bottom gate architecture of a TFT device with PEDOT:PSS as the active layer, PAH/PAA as the gate dielectric layer, silver as the source and drain electrodes, and aluminum as the gate electrode.
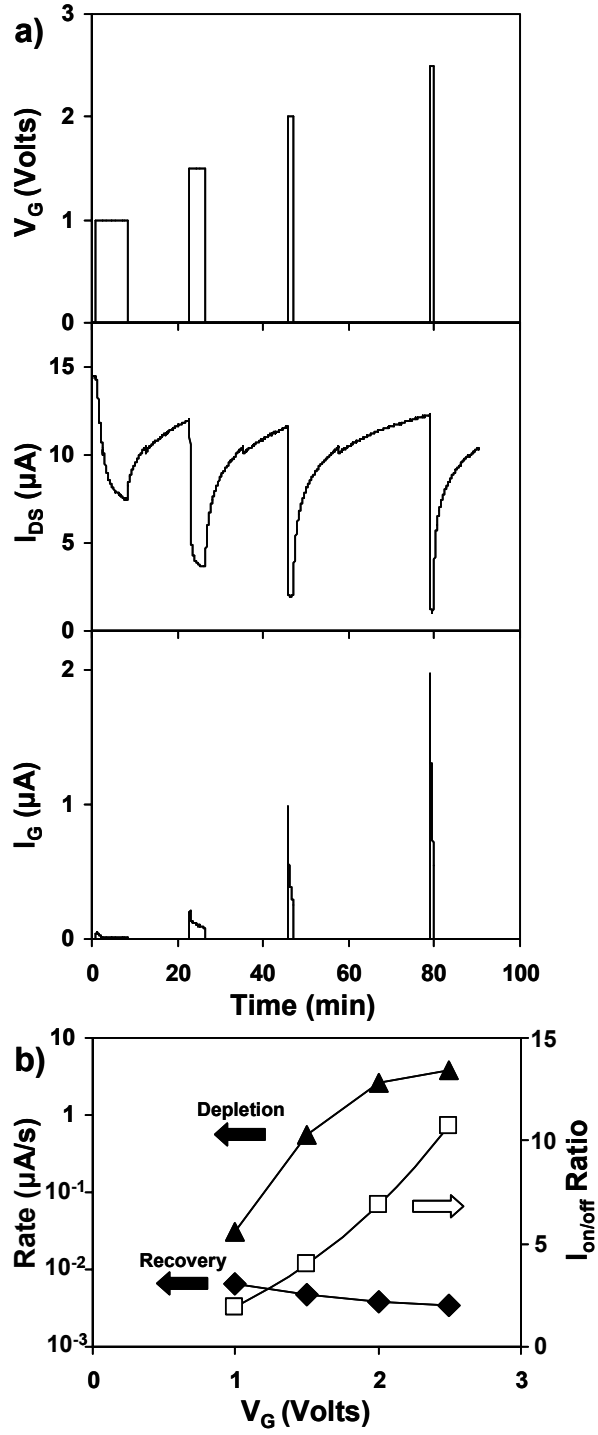
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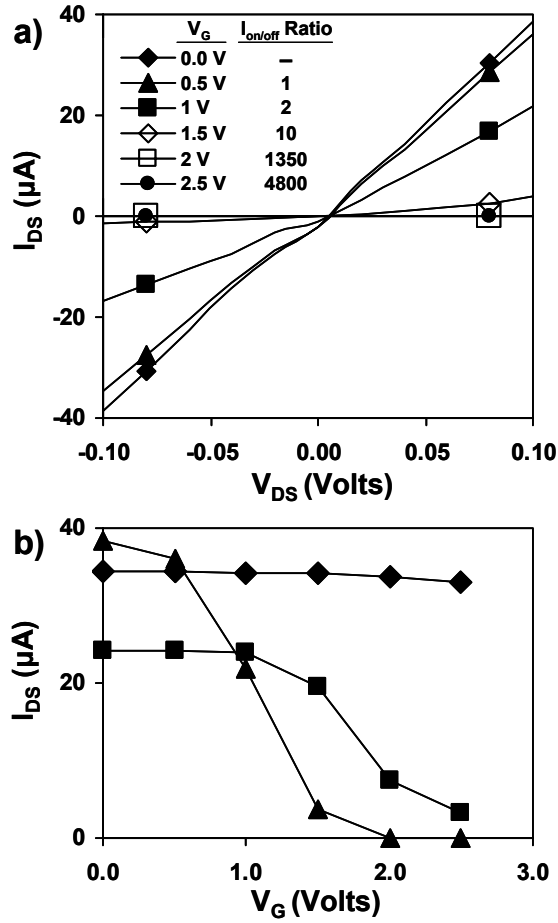under ambient conditions with the application of a 2.0 V gate bias.

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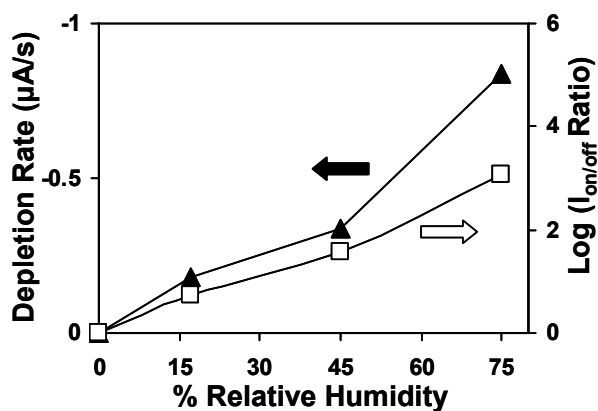
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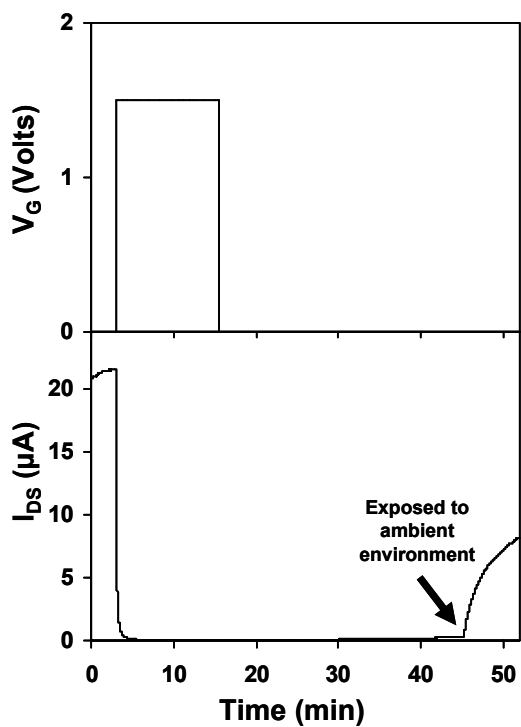
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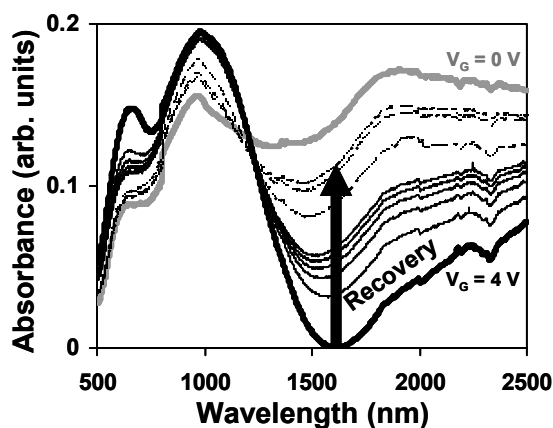
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